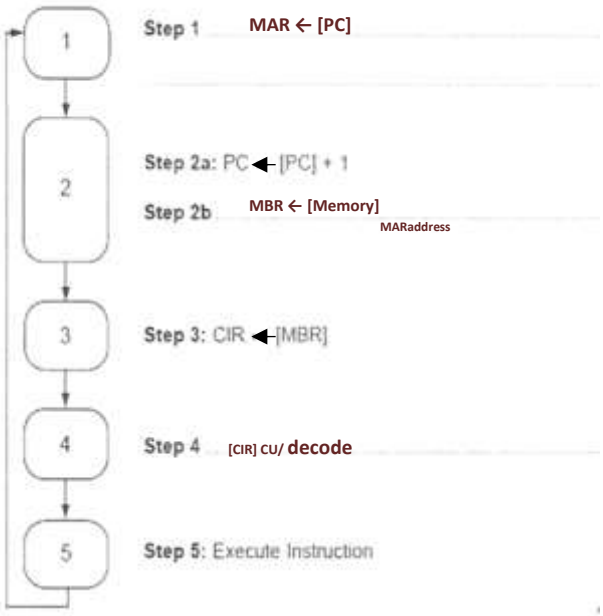
Answer

1 (a) State the full names of 3 registers that are used in the fetch part of the fetch-decode execute cycle.
Register 1 MAR
Register 2 MDR/MBR
Register 3 CIR/IR [3]

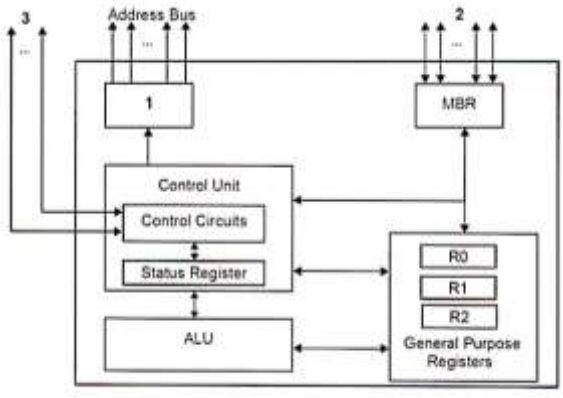
(b) Figure 1 below is an incomplete diagram of the fetch-decode- execute cycle. Describe the missing steps 1, 2b and 4 using either register transfer notation or written description. 2 Steps 2a and 2b occur at the same time. [3]

Figure 1



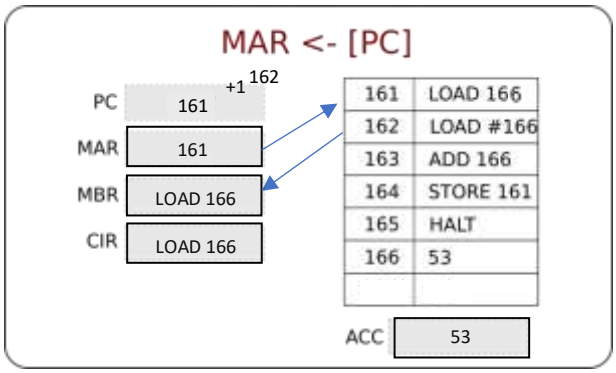
2) Figure 2 below shows an incomplete diagram of the components of a processor.

Provide full names for the components numbered 1 to 3 in Figure 2 by completing the table below.



Component Number	Component Name
1	MAR
2	Data bus
3	Control bus

3) Complete the following diagrams showing each step of the fetch decode execute cycle. Draw the necessary buses



4) Write an assembly language program C = (num1 - num2) + num3;

```
INP
STA 23
INP
STA 24
INP
STA 25
LDA 23
SUB 24
ADD 25
OUT
HLT
DAT
```