

Formative Assessment 1

Name _____

- 1) Von Neumann Architecture is divided into
 - A. 5 parts
 - B. 2 parts
 - C. 7 parts
 - D. 4 parts

- 2) Von Neumann architecture includes:
 - A. Registers, Memory, Input device, Output device
 - B. CPU, Memory, Input device, Output device
 - C. ALU, CU, Memory, Input devices, Output devices

- 3) The processor is divided into:
 - A. ALU /CU/ Register
 - B. MAR/ALU/CU
 - C. ALU /CU/ Memory Unit
 - D. ALU /CU/ BUS

- 4) Main memory, Input and Output devices are connected to the processor using the following buses:
 - A. Control bus, System bus
 - B. Control bus, Data bus, Address bus
 - C. Data bus, Address bus, System bus

- 5) Operations of ALU, Input, Output, Memory are controlled by
 - A. System bus
 - B. Data Bus
 - C. Control Unit
 - D. Registers

- 6) ALUs perform all:
 - A. Arithmetic operations
 - B. Arithmetic and Boolean operations
 - C. Main operations
 - D. Control operations

- 7) The control bus consists of signals that permit the CPU to communicate with the...
 - A. Memory and I/O devices
 - B. I/O devices
 - C. ALU and CU

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- 1) Von Neumann Architecture is divided into
 - A. 5 parts
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- 2) Von Neumann architecture includes:
 - D. Registers, Memory, Input device, Output device
 - E. CPU, Memory, Input device, Output device
 - F. ALU, CU, Memory, Input devices, Output devices

- 3) The processor is divided into:
 - E. ALU /CU/ Register
 - F. MAR/ALU/CU
 - G. ALU /CU/ Memory Unit
 - H. ALU /CU/ BUS

- 4) Main memory, Input and Output devices are connected to the processor using the following buses:
 - D. Control bus, System bus
 - E. Control bus, Data bus, Address bus
 - F. Data bus, Address bus, System bus

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