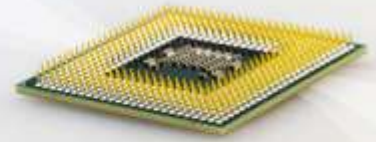


# Von Neumann architecture

11.1A Computer systems

# Learning objectives



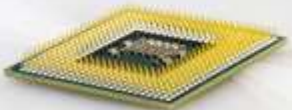
- describe the interaction of CPU with peripheral devices
- describe the purpose of CPU components, system bus and main memory

## ASSESSMENT CRITERIA

- Explain how CPU connected with peripherals
- Describe the purpose of CU, ALU
- Describe the pupose of system bus

## Key Words

Control bus	is used to provide control signals to most parts of a computer system.
Address bus	is used to address the main system memory
Data bus	Is used to transfer data
Peripherals	devices that can be easily removed and plugged into a computer system.



## What is a computer?

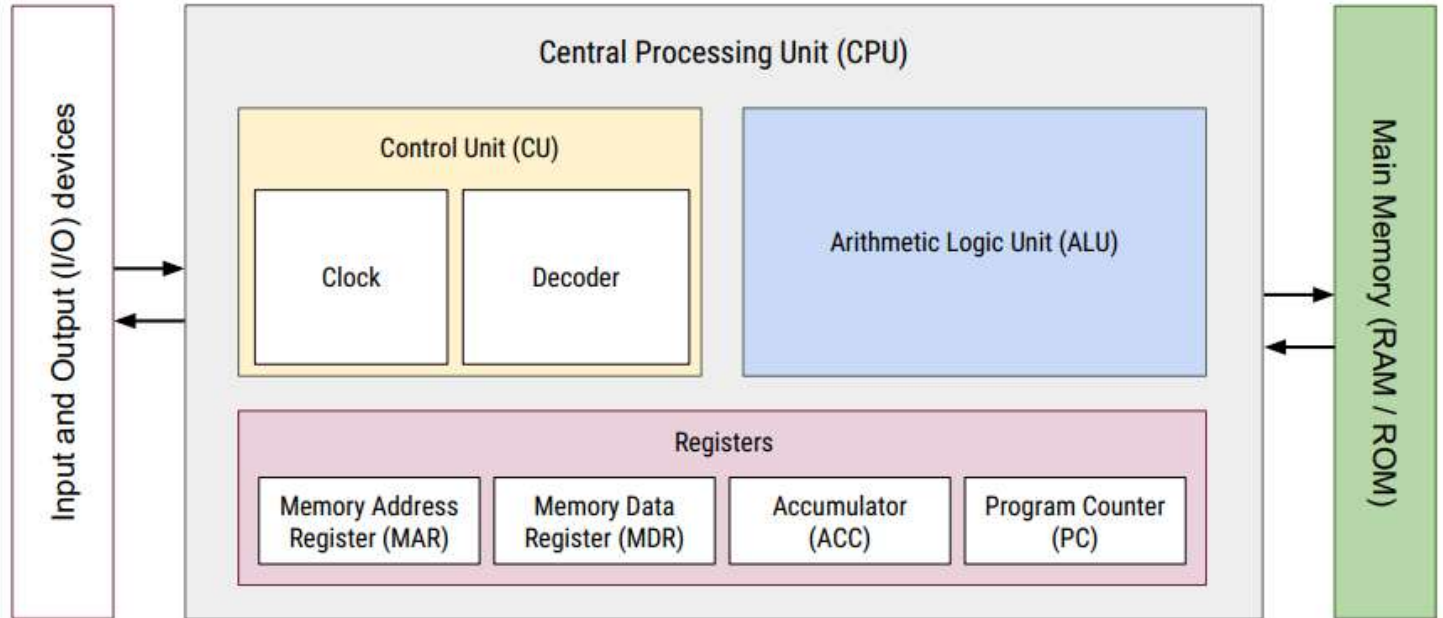


### Program

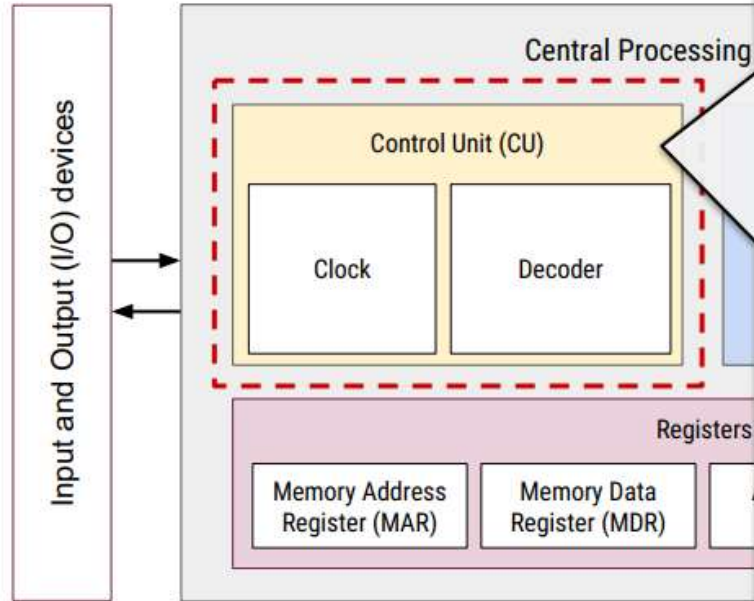
- 5       $\longrightarrow$
1. Input number
  2. Multiply number by itself
  3. Output number       $\longrightarrow$       25
  4. End



# The Von Neumann CPU architecture



# The Von Neumann CPU architecture



## The Control Unit (CU)

- The purpose of the Control Unit is to **execute instructions** and send **control signals** to other components within the CPU
- The Control Unit contains two main components - the **decoder** and the **clock**
- The **clock** sends an electrical pulse at a fixed interval to **synchronise activity** between components within the CPU
- The decoder **decodes instructions** that are **retrieved from memory** during the fetch-execute cycle



# The Von Neumann CPU architecture

## The Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) performs all of the **arithmetic** (mathematical) and **logical** operations of the CPU, including:

- Addition and subtraction, multiplication and division
- Relational operations (comparison) such as whether numbers are equal or if one is greater than another
- Boolean logic operations such as AND, OR and NOT

The results of operations by the ALU are stored in the **Accumulator** register.

## Central Processing Unit (CPU)

Arithmetic Logic Unit (ALU)

## Registers

Accumulator  
(ACC)

Program Counter  
(PC)

Main Memory (RAM / ROM)



# Dedicated registers

**Memory Address Register (MAR)** – The address in main memory that we wish to fetch the instruction from

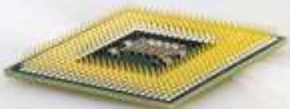
**Memory Buffer Register (MBR)** – Holds the instruction that has been fetched from memory

**Current instruction register (CIR)** – Holds the contents of MBR, which is the instruction to be processed

**Program Counter (PC)** – This holds the memory address of the location to fetch the next instruction from.

**Status Register (SR)** – Gives information on such things as overflow/underflow, interrupts, parity. The status register allows an instruction to depend the outcome of the previous instruction.

**Accumulator** – Holds the results of arithmetic and logic computations





# Exam style questions

5 Most modern computers are designed using Von Neumann architecture. (a)  
Describe what is meant by Von Neumann architecture. ....

.....  
.....  
.....  
.....  
.....[2]



## Answer

- 5 (a) a single processor 1  
program consists of a sequence of stored instructions 1  
instructions + data make up a 'program' 1  
are stored in a continuous block of main memory 1  
instructions are executed in sequence 1 [max 2]



# Question

3 A computer is designed using the Von Neumann model. (a) Describe the role of the Arithmetic and Logic Unit (ALU) and Control Unit

(ALU) in the Von Neumann model. ALU.....  
.....  
.....  
.....  
.....

CU.....  
.....  
.....  
.....[4]



## Answer

3(a)	<p><b>1 mark</b> per bullet to <b>max 2</b> for each group</p> <ul style="list-style-type: none"><li>• <b>ALU</b> performs arithmetic operations</li><li>• And logical operations / comparisons</li> <li>• <b>Control Unit</b> sends / receives signals</li><li>• Synchronises operations</li><li>• to control operations // execution of instructions</li><li>• Accept by example e.g. Input output // flow of data</li></ul>	<b>4</b>
------	--	----------



8 The Von Neumann model uses a series of registers. (a) Explain what is meant by the term register. ....

.....  
.....  
.....  
.....[2]

8(a)	<b>1 mark per bullet to max 2</b> <ul style="list-style-type: none"><li>• Small piece / word of (fast) memory</li><li>• Part of the processor</li><li>• Temporary storage of data</li><li>• Data is about to be / has been processed</li></ul>	<b>2</b>
------	--	----------



6 (a) Describe the stored program concept for the basic Von Neumann model for a computer system.

.....  
.....  
.....  
.....[3]

6 (a) Any **three** from:

- program must be resident in (main) memory to be executed
- program consists of a sequence of instructions
- which occupy a (contiguous) block of main memory
- instructions and data are indistinguishable
- each instruction is fetched, (decoded) and then executed
- instruction fetch and data operation cannot occur at the same time

[3]

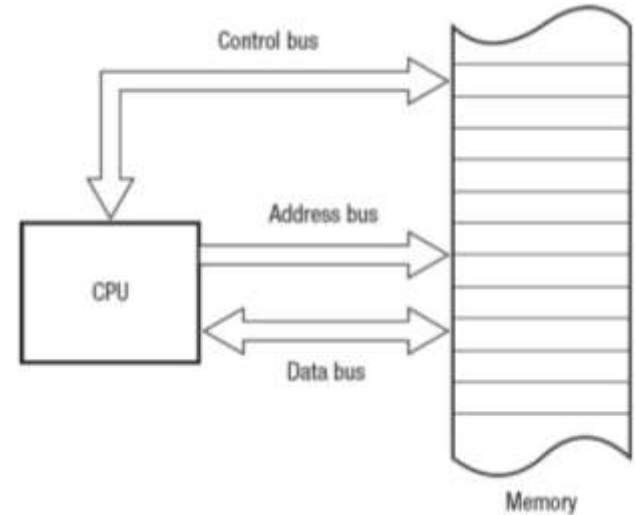


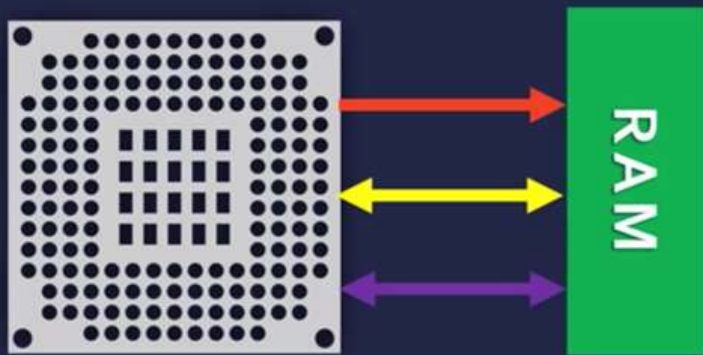
# Buses

[https://www.youtube.com/watch?v=3osm-soT\\_Lc](https://www.youtube.com/watch?v=3osm-soT_Lc)

**Bus** = a collection of wires through which data is transmitted

**Buses** are groups of parallel microscopic wires that connect the processor to the various input and output controllers being used by the computer. They are also used to connect the internal components of a microprocessor, known as **registers** and to connect the microprocessor to memory. There are three types of bus: data, address and control.





- Can be unidirectional or bidirectional
- 3 types of bus:

- An **address bus** sends a memory address along the bus from the CPU to the memory. To fetch/write data, the CPU needs to tell the RAM the address
- A **data bus** sends the actual data to and from the memory.
- A **control bus** carries commands from the CPU and status messages from other hardware devices.





# Peripherals



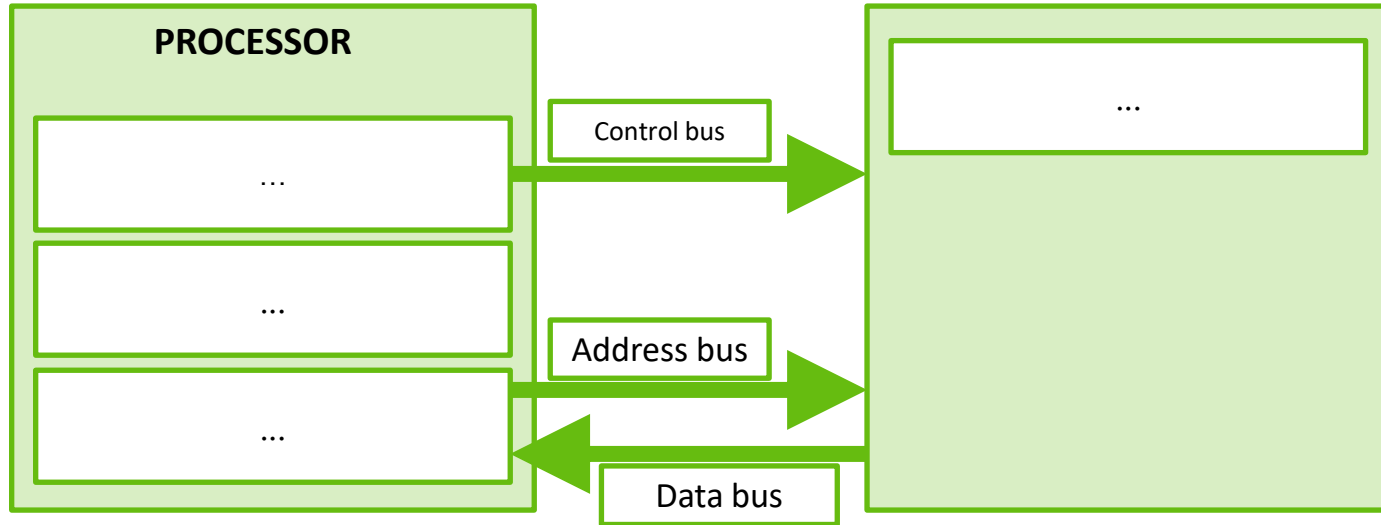
A computer device that is not part of the CPU is called a peripheral or preripheral device. It can be external (e.g. mouse, keyboard, printer, monitor, memory stick) or internal, such as a CD-ROM drive. The system bus is not connected directly to I/O devices, it is connected to an I/O controller then the I/O controller is connected to the I/O device. I/O controller – an electronic circuit that connects a system bus and peripherals. It provides the correct voltages and currents for the system bus and peripheral devices.



# ACTIVITY-2 (PARTS OF the CPU)

1. Use the labels below to complete the diagram.

- Memory
- Control unit
- Arithmetic and logic unit (ALU)
- Registers



# Activity-3

Using your diagram from the previous activity, complete the table below by identifying the name of each bus from the description:

Description	Name
Sends and receives signals that control the CPU and other parts of the computer system.	
Carries the address of memory locations used to store data and program instructions.	
Transfers the binary data around the computer.	

# A Level questions

(a) Name and describe **three** buses used in the von Neumann model.

Bus 1 .....

Description .....

.....

.....

Bus 2 .....

Description .....

.....

.....

Bus 3 .....

Description .....

.....

.....



# Answers

(a) **one mark** for name of bus + **one mark** for description

## **address bus**

- lines used to transfer address of memory or input/output location
- unidirectional bus

## **data bus**

- used to transfer data between the processor and memory/input and output devices
- bidirectional bus

## **control bus**

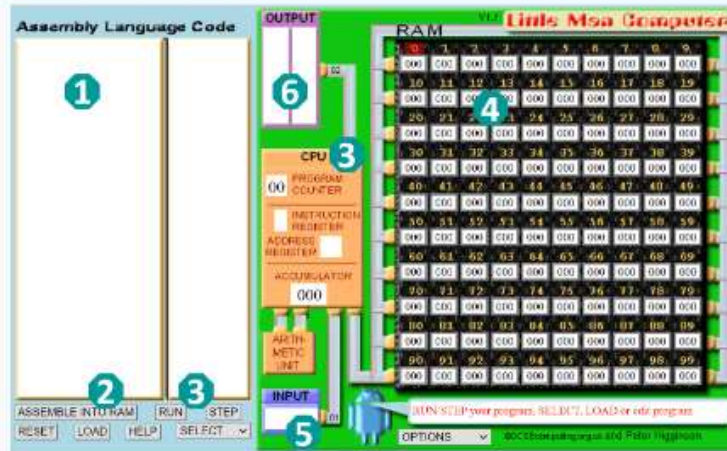
- used to transmit control signals
- e.g. read/write/fetch/ ...
- dedicated bus since all timing signals are generated according to control signal

[6]



# Practice work

## LMC



1 - space for a typing program

2 - button of compiling the program

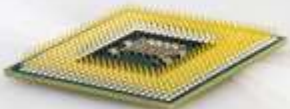
3 - button RUN the whole program, STEP - line by line

4 - registers of CPU

5 - the memory location

6 - input data

7 - output data



LMC contains a set of commands called mnemonics.

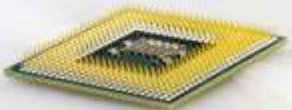
Mnemonic Code	Numeric Code XX is the cell number in the memory compartment.	Instruction
INP	901	Input data
OUT	902	Output data
ADD	1XX	Add data
SUB	2XX	Subtract data
STA	3XX	Store data
LDA	5XX	Load data
BRA	6XX	Branch to a specified cell
BRZ	7XX	If 0, branch to a specified cell
BRP	8XX	If 0 or positive, branch to a specified cell
HLT	000	Break execution
DAT		Treat content as data



## Task 1

Write a program that asks for a number and prints it out.

```
00 INP    input number to accumulator
01 STA 06 store number from the accumulator to a memory location (address) 10
02 OUT    output number from the accumulator
03 HLT    stop program
```





## Task 2

Write a program that stores a pair of numbers in variables called FIRST and SECOND. The two numbers should be added together. The answer should be stored in a variable called ANSWER and then output.

```
00 INP          input 1st number to accumulator
01 STA FIRST    store number from the accumulator to a memory location (address) FIRST (08)
02 INP          input 2nd number to accumulator
03 STA SECOND   store number from the accumulator to a memory location (address) SECOND (09)
04 ADD FIRST    add a number from memory location FIRST (9) to number in the accumulator
05 STA ANSWER   store number from the accumulator to a memory location (address) ANSWER (10)
06 OUT          output number from the accumulator
07 HLT          stop program
08 FIRST DAT
09 SECOND DAT
10 ANSWER DAT
```

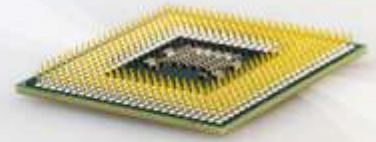


## Extra tasks

[https://starwort.github.io/computer-science/Paper\\_1/lmc/wfh/term\\_5/week\\_3/lmc\\_tasks.html](https://starwort.github.io/computer-science/Paper_1/lmc/wfh/term_5/week_3/lmc_tasks.html)



# Learning objectives



- describe the interaction of CPU with peripheral devices
- describe the purpose of CPU components, system bus and main memory

## ASSESSMENT CRITERIA

- Explain how CPU connected with peripherals
- Describe the purpose of CU, ALU
- Describe the pupose of system bus



# Lesson Feedback



**3**

3 things you  
have learned  
today

**2**

2 things were  
interesting for  
you

**1**

1 thing I want  
to learn more